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Substitute for form 1448A/PTO				<b>Complete if Known</b>	
<b>INFORMATION DISCLOSURE STATEMENT BY APPLICANT</b>  (Use as many sheets as necessary)				Application Number	10/608,287
				Filing Date	June 27, 2003
				First Named Inventor	Yeo, et al.
				Art Unit	2891
				Examiner Name	Chaudhari, Chandra P.
Sheet	1	of	4	Attorney Docket Number	TSM03-0421

U.S. PATENT DOCUMENTS					
Examiner Initials*	Cite No. <sup>1</sup>	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number - Kind Code <sup>2</sup> (if known)			
CC	1	US-4,933,298	06-12-1990	Hasegawa	
	2	US-4,948,799	08-07-1990	Blake et al.	
	3	US-5,317,175	05-31-1994	Throngnumachai	
	4	US-5,317,178	05-31-1994	Wu	
	5	US-5,464,783	11-07-1995	Kim et al.	
	6	US-5,607,865	03-04-1997	Choi et al.	
	7	US-5,814,895	09-29-1998	Hirayama	
	8	US-5,998,852	12-07-1999	Berry et al.	
	9	US-6,114,725	09-05-2000	Furukawa et al.	
	10	US-6,157,061	12-05-2000	Kawata	
	11	US-6,222,234 B1	04-24-2001	Imai	
	12	US-6,300,182 B1	10-09-2001	Yu	
	13	US-6,342,410 B1	01-29-2002	Yu	
	14	US-2002/0011612 A1	01-31-2002	Hieda	
	15	US-6,344,392 B1	02-05-2002	Liaw	
	16	US-6,380,024 B1	04-30-2002	Liaw	
	17	US-6,387,739 B1	05-14-2002	Smith, III	
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	19	US-6,411,725 B1	06-25-2002	Rhoads	
	20	US-6,475,869 B1	11-05-2002	Yu	

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Examiner Initials*	Cite No.	Foreign Patent Document	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T <sup>6</sup>
		Country Code <sup>3</sup> - Number <sup>4</sup> - Kind Code <sup>5</sup> (if known)				
CC	21	JP 02-015675	01-19-1990	Fujitsu LTD		
CC	22	FR 2 617 642	01-06-1989	Thomson Semiconducteurs		

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				Art Unit	2891
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CC	23	US-6,475,890 B1	11-05-2002	Yu	
	24	US-6,476,437 B2	11-05-2002	Liaw	
	25	US-2003/0011080 A1	01-16-2003	Deshpande et al.	
	26	US-6,514,808 B1	02-04-2003	Samavedam et al.	
	27	US-6,521,949 B2	02-18-2003	Assaderaghi et al.	
	28	US-2003/0042528 A1	03-08-2003	Forbes	
	29	US-6,534,807 B2	03-18-2003	Mandelman et al.	
	30	US-6,573,549 B1	08-03-2003	Deng et al.	
	31	US-2003/0111878 A1	06-19-2003	Colombo et al.	
	32	US-2003/0113970 A1	06-19-2003	Fried et al.	
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	35	US-6,611,029 B1	08-26-2003	Ahmed et al.	
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Examiner Signature	Chandra Chaudhari	Date Considered	9-05
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		Application Number	10/608,287		
		Filing Date	June 27, 2003		
		First Named Inventor	Yeo, et al.		
		Art Unit	2891		
		Examiner Name	Chaudhari, Chandra P.		
Sheet	3	of	4	Attorney Docket Number	TSM03-0421

NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T <sup>2</sup>
CC	48	AUTH, C.P., et al., "Scaling Theory for Cylindrical, Fully-Depleted, Surrounding-Gate MOSFET's," IEEE Electron Device Letters, Vol. 18, No. 2 (February 1997) pp. 74-76.	
↓	49	CELIK, M., et al., "A 45 nm Gate Length High Performance SOI Transistor for 100nm CMOS Technology Applications," Symposium on VLSI Technology Digest of Technical Papers (2002) pp. 166-167.	
	50	CHAU, R., et al., "A 50nm Depleted-Substrate CMOS Transistor (DST)," IEDM (2001) pp. 621-624.	
	51	CHEN, W., et al., "Suppression of the SOI Floating-Body Effects by Linked-Body Device Structure," Symposium on VLSI Technology Digest of Technical Papers (1996) pp. 92-93.	
	52	FUNG, S.K.H., et al., "Gate Length Scaling Accelerated to 30nm Regime Using Ultra-Thin Film PD-SOI Technology," IEDM (2001) pp. 629-632.	
	53	GEPPERT, L., "The Amazing Vanishing Transistor Act," IEEE Spectrum (October 2002) pp. 28-33.	
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	55	JE, M., et al., "Quantized Conductance of a Gate-All-Around Silicon Quantum Wire Transistor," Microprocesses and Nanotechnology Conference (1998) pp. 150-151.	
↓	56	NEMATI, F., et al., "A Novel Thyristor-Based SRAM Cell (T-RAM) for High-Speed, Low-Voltage, Giga-Scale Memories," IEDM (1999) pp. 283-286.	
	57	NITAYAMA, A., et al., "Multi-Pillar Surrounding Gate Transistor (M-SGT) for Compact and High-Speed Circuits," IEEE Transactions on Electron Devices, Vol. 38, No. 3 (March 1991) pp. 579-583.	
	58	OH, S-H., et al., "Analytic Description of Short-Channel Effects in Fully-Depleted Double-Gate and Cylindrical, Surrounding-Gate MOSFETs," IEEE Electron Device Letters, Vol. 21, No. 9 (September 2000) pp. 445-447.	

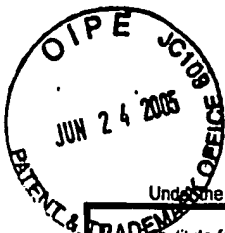
Examiner Signature	Chandra Chaudhari	Date Considered	9-05
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CC	59	SATO, N., et al., "Hydrogen Annealed Silicon-On-Insulator," Appl. Phys. Lett., Vol. 65, No. 15 (October 10, 1994) pp. 1924-1926.	
CC	60	SHAHIDI, G.G., "SOI Technology for the GHz Era," IBM J. RES. & DEV., Vol. 46, No. 2/3 (March/May 2002) pp. 121-131.	
CC	61	TANG, S.H., et al., "FinFET - A Quasi-Planar Double-Gate MOSFET," IEEE International Solid-State Circuits Conference (2001) pp. 118-119 & 437.	
CC	62	YAMAGATA, K., et al., "Selective Growth of Si Crystals from the Agglomerated Si Seeds over Amorphous Substrates," Appl. Phys. Lett., Vol. 61, No. 21 (November 23, 1992) pp. 2557-2559.	

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